Lecture 8 – 06/11/2024

The *p-n* junction

- Basic considerations
- At thermal equilibrium
- Space charge region

Summary Lecture 7

Carrier mobility at <u>low</u> electric field

$v_d = \mu_0 E$

$\mu_0 \dots$ low field mobility

$$\frac{1}{\mu_0} = \frac{1}{\mu_{\mathrm{LA}}} + \frac{1}{\mu_{\mathrm{LO}}} + \frac{1}{\mu_{\mathrm{ion}}} + \cdots$$ Matthiessen rule

Carrier mobility at <u>high</u> electric field

$$v_d = \mu_0 E \sqrt{\frac{T}{T_e}}$$

T_e ... Carriers' effective temperature
T ... Lattice (phonon) temperature

$$\frac{T_e}{T} = \frac{1}{2}\left[1 + \sqrt{1 + \frac{3\pi}{8}\left(\frac{\mu_0 E}{c_s}\right)}\right]$$

c_s ... velocity of sound

$$v_s = \sqrt{\frac{8E_{ph}}{3\pi m^*}} \approx 10^7 \text{ cm/s}$$

v_s ... saturation velocity
E_{ph} ... optical-phonon energy

Out of equilibrium semiconductors

$pn \neq n_i^2$ due to excess carriers injected by electrical or optical means

$$\frac{\partial n}{\partial t} = G - R + \left(\frac{1}{e}\right)\nabla \cdot \mathbf{J_n}$$

$$\frac{\partial p}{\partial t} = G - R - \left(\frac{1}{e}\right)\nabla \cdot \mathbf{J_p}$$

continuity equations for electrons/holes

$$G = G_{th} + G_L$$

processes to restore equilibrium $(pn = n_i^2)$:

$pn > n_i^2 \dots$ recombination, rate R

$pn < n_i^2 \dots$ thermal generation, rate G_{th}

Summary Lecture 7

Band-to-band recombination – photon emission

Far more probable in direct-bandgap SCs

weak to moderate injection ($\leq 10^{18}\ \mathrm{cm}^{-3}$):

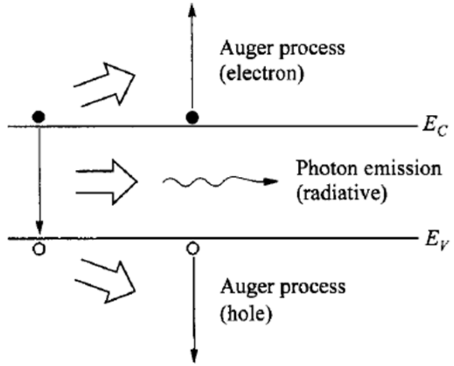
$$R - G_{th} = \begin{cases} 0 & \text{thermal equilibrium} \\ \dfrac{n - n_0}{\tau_n} & p\text{-type} \quad p \approx p_0 \\ \dfrac{p - p_0}{\tau_p} & n\text{-type} \quad n \approx n_0 \end{cases}$$

Band-to-band recombination – Auger-Meitner process

At play in both direct- and indirect-bandgap SCs

high injection ($> 10^{18}\ \mathrm{cm}^{-3}$):

$$R_A - G_{th} \propto \begin{cases} p^2 n & p\text{-type} \quad p \approx \Delta p \\ n^2 p & n\text{-type} \quad n \approx \Delta n \end{cases}$$



Single-level recombination – traps

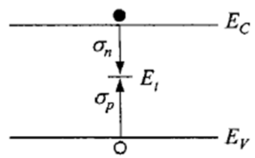
Dominating at low injection in both direct- and indirect-bandgap SCs

(1) electron capture from CB
(2) electron emission to CB
(3) hole capture from VB
(4) hole emission to VB

$$\frac{dn}{dt} = G_L + R_n = G_L + r_{e,n} - r_{c,n}$$

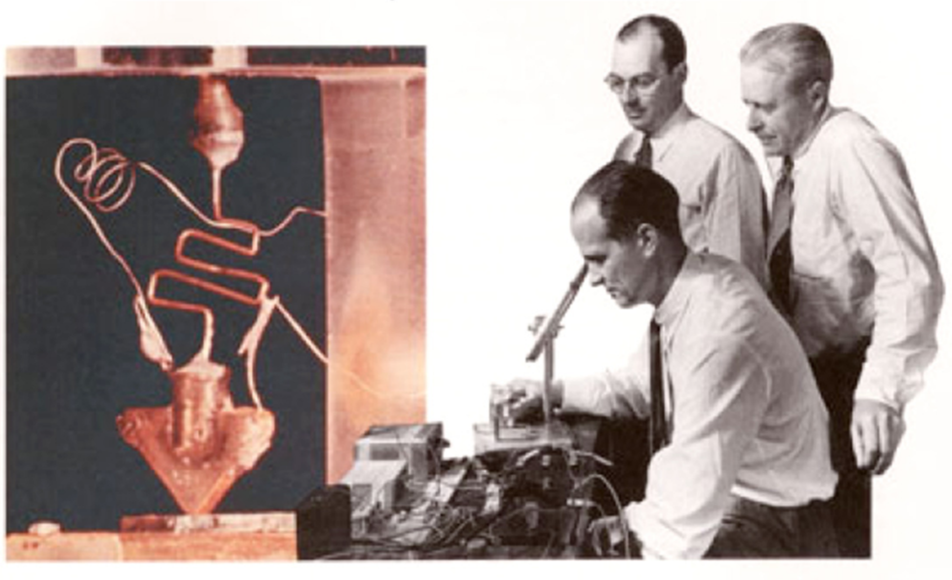
$$R_n = r_{e,n} - r_{c,n} = v_{th}\sigma_n(nN_t^{\times} - n_t N_t^{-})$$

$$N_t^{\times} = N_t(1 - f), \quad N_t^{-} = N_t f$$



1st *p-n* junction and 1st transistor (1947)

First transistor Bardeen, Shockley and Brattain 1947



1939

Nobel prize in physics 1956

Point contact transistor

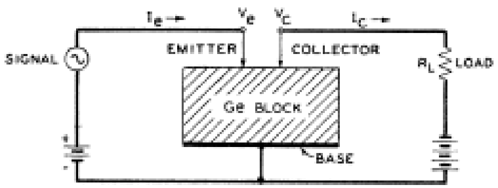
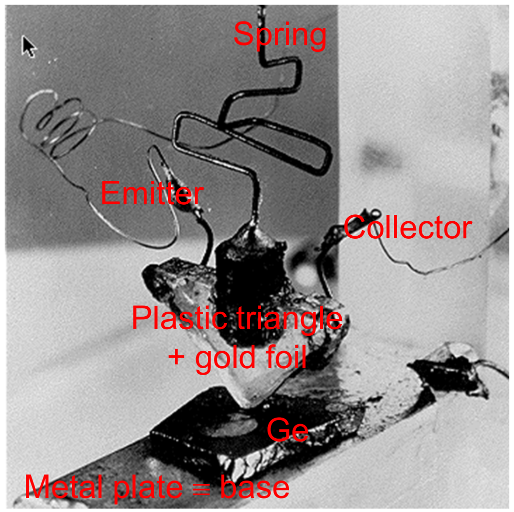


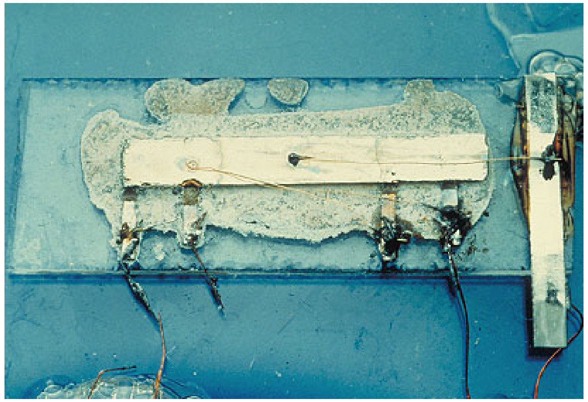
FIG. 1. Schematic of semi-conductor triode.

J. Bardeen and W. H. Brattain, Phys. Rev. **74**, 230 (1948)

> 520 citations

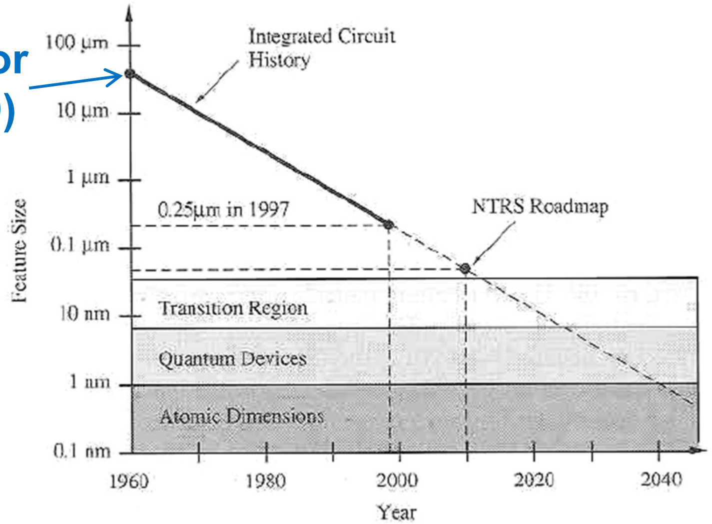


Transistor: past... and ...future

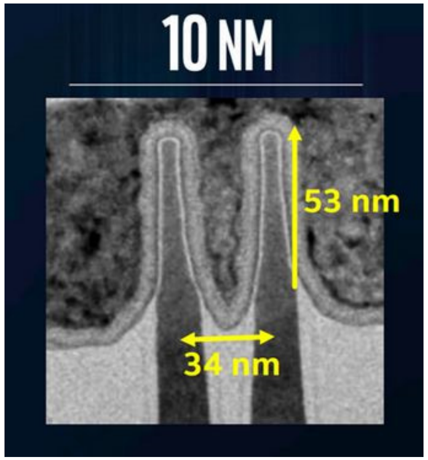


First integrated circuit (few transistors)
Jack Kilby, TI - 1958 – Nobel prize (2000)
Dimension: 11 × 1.6 mm²

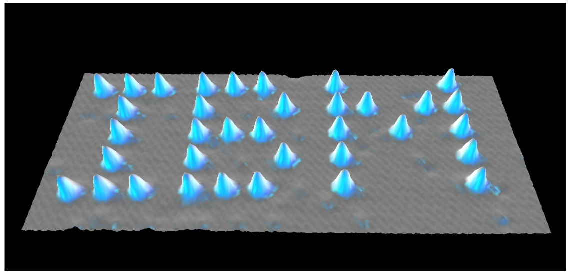
CMOS transistor invention (1960)

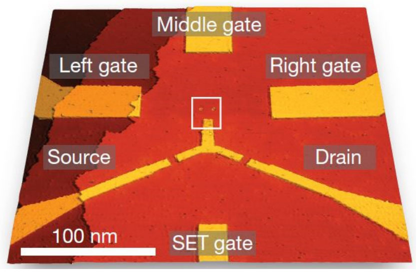


National technology roadmap for semiconductors (NTRS)
Now ITRS (I: international)



Intel 10 nm process node

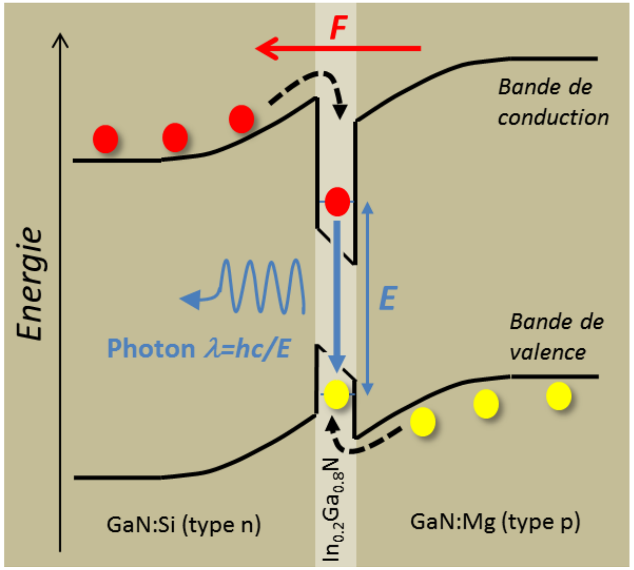




Y. He *et al*., Nature **571**, 371 (2019)
> 230 citations

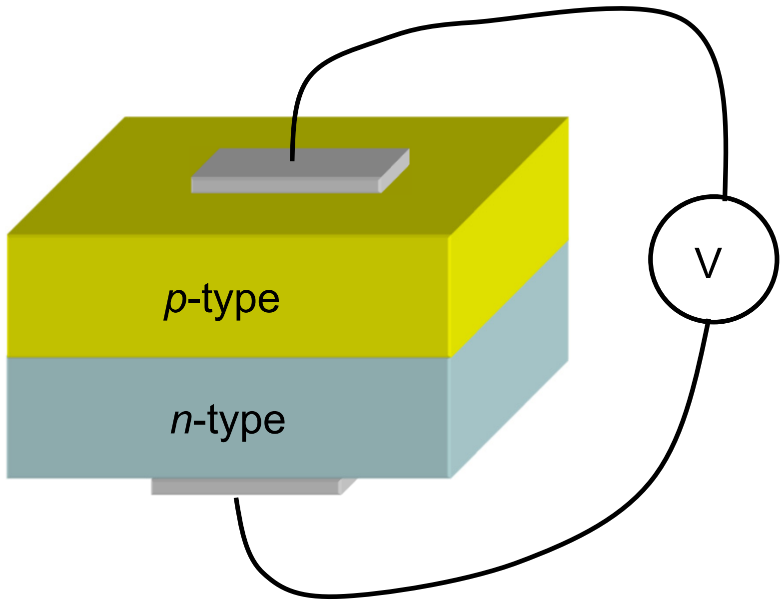
Some applications

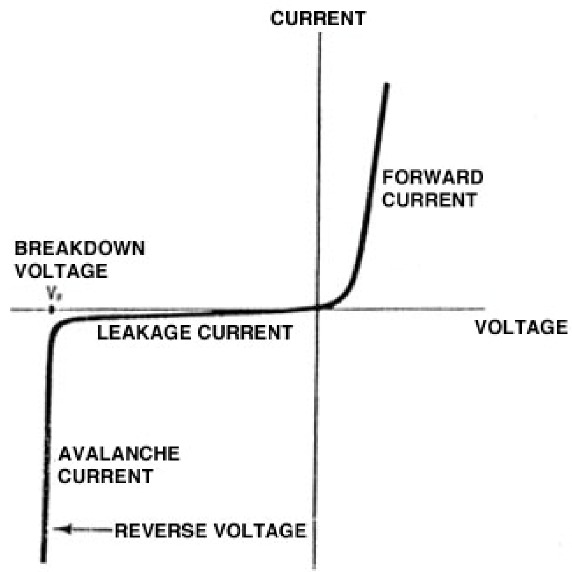
- Bipolar transistors
- LEDs
- Laser diodes
- Solar cells
- Photodetectors



p-*n* junction (2D-geometry)

Made of two adjacent semiconductor layers which are *p*-type and *n*-type doped





A p-n junction behaves like a diode (rectifying behavior)

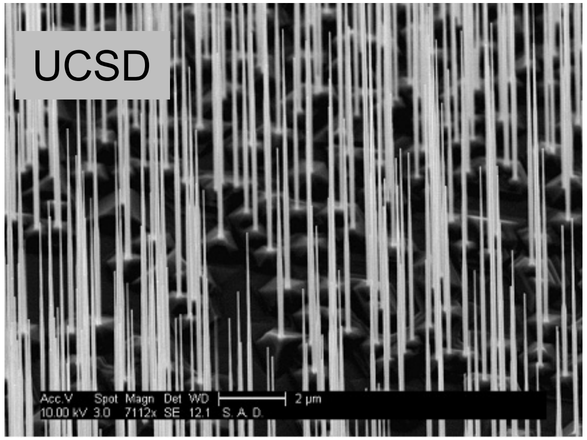
Early historical account detailed in: W. Shockley, Bell Syst. Tech. J. **28**, 435 (1949); C.-T. Sah, R. N. Noyce, and W. Shockley, Proc. IRE **45**, 1228 (1957) > 1600 citations

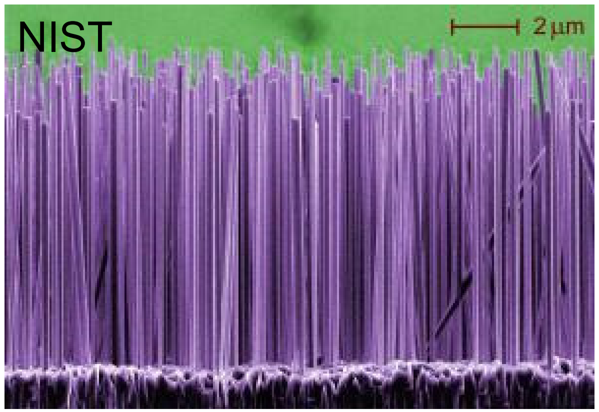
> 2200 citations

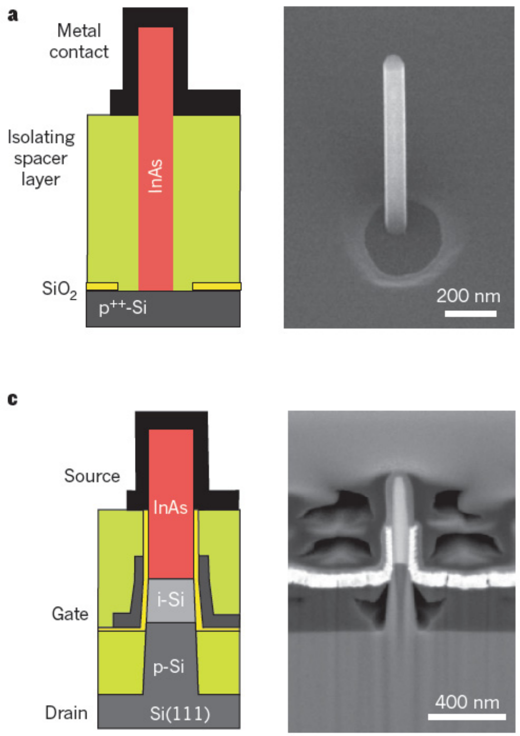
p-n junction (research, nanowire geometry)

Semiconductor nanowires (candidates for tunnel-FETs)

Subthreshold swing < 60 mV/decade at 300 K
(cf. forthcoming Lecture 9)



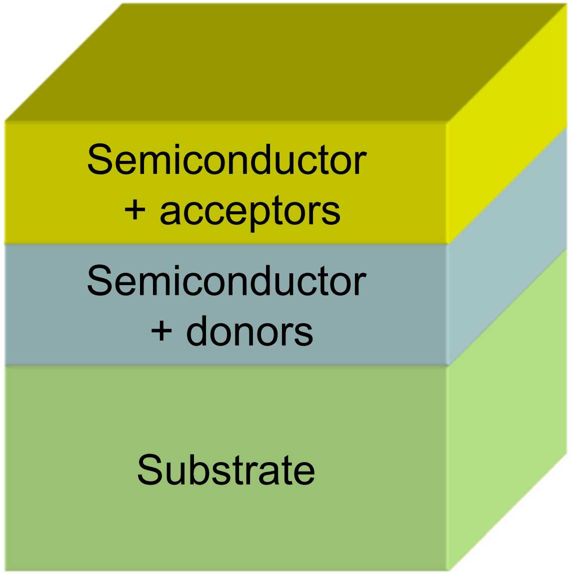


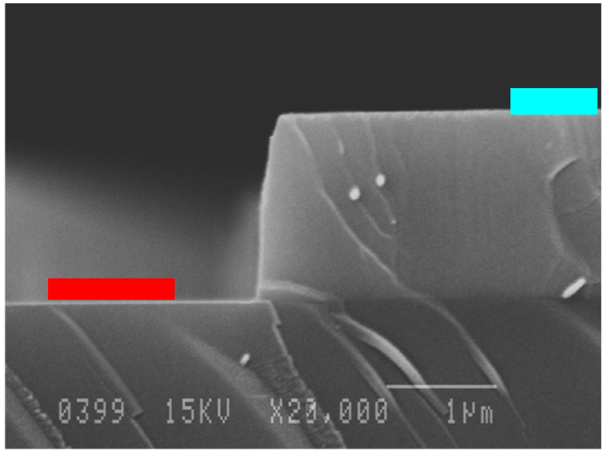


A. M. Ionescu and H. Riel, Nature **479**, 329 (2011)
> 2200 citations

p-n junction fabrication

During growth by impurity incorporation

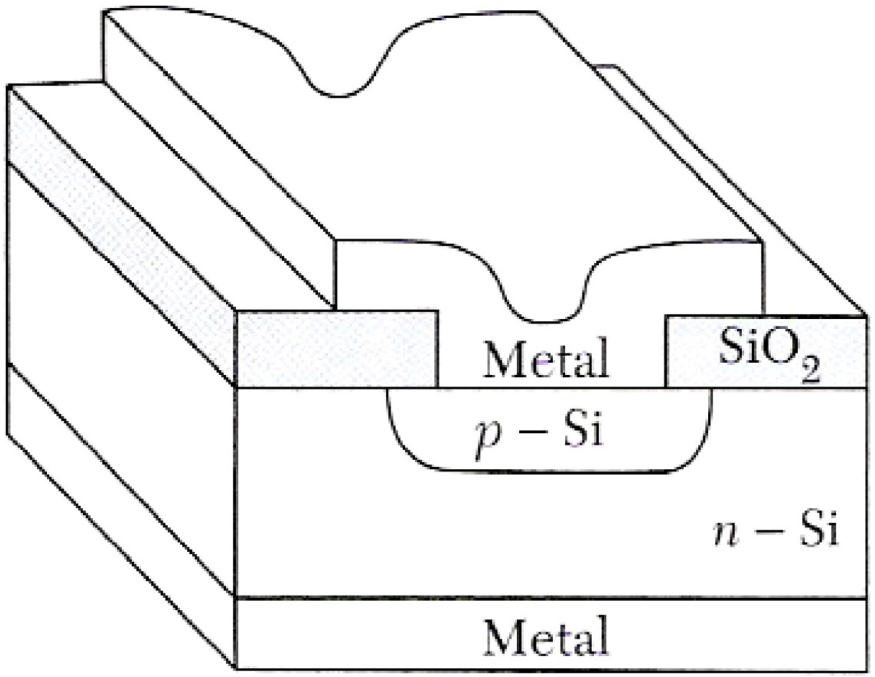




SEM image of a *p*-*n* junction (LED)

p-n junction fabrication

Post-growth: by impurity diffusion or implantation



p-n junction fabrication

Post-growth: by impurity diffusion or implantation

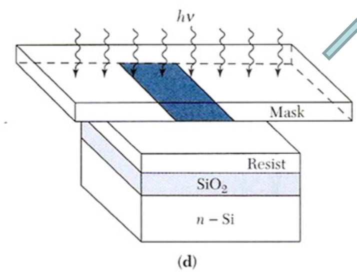


Fig. 1 (*a*) A bare *n*-type Si wafer. (*b*) An oxidized Si wafer by dry or wet oxidation. (*c*) Application of resist. (*d*) Resist exposure through the mask.

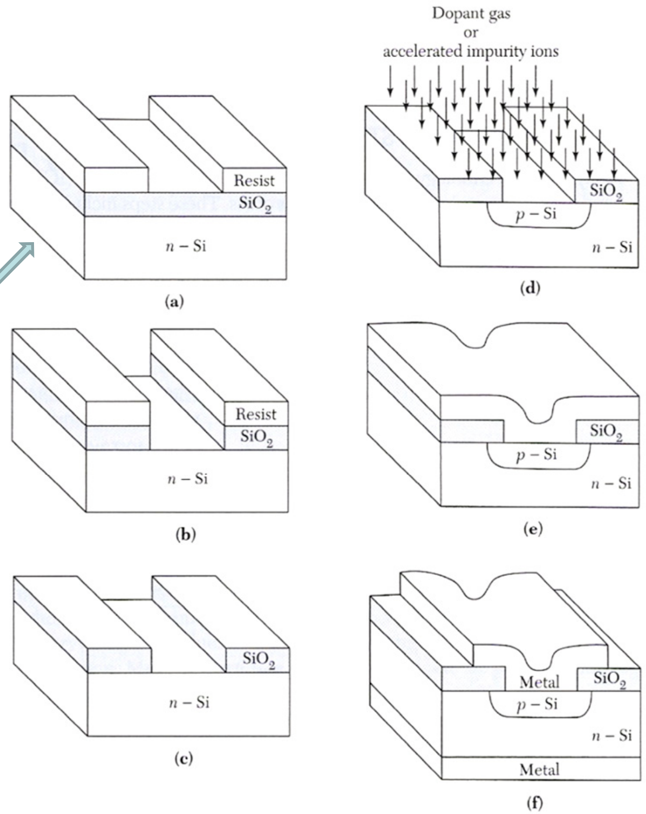
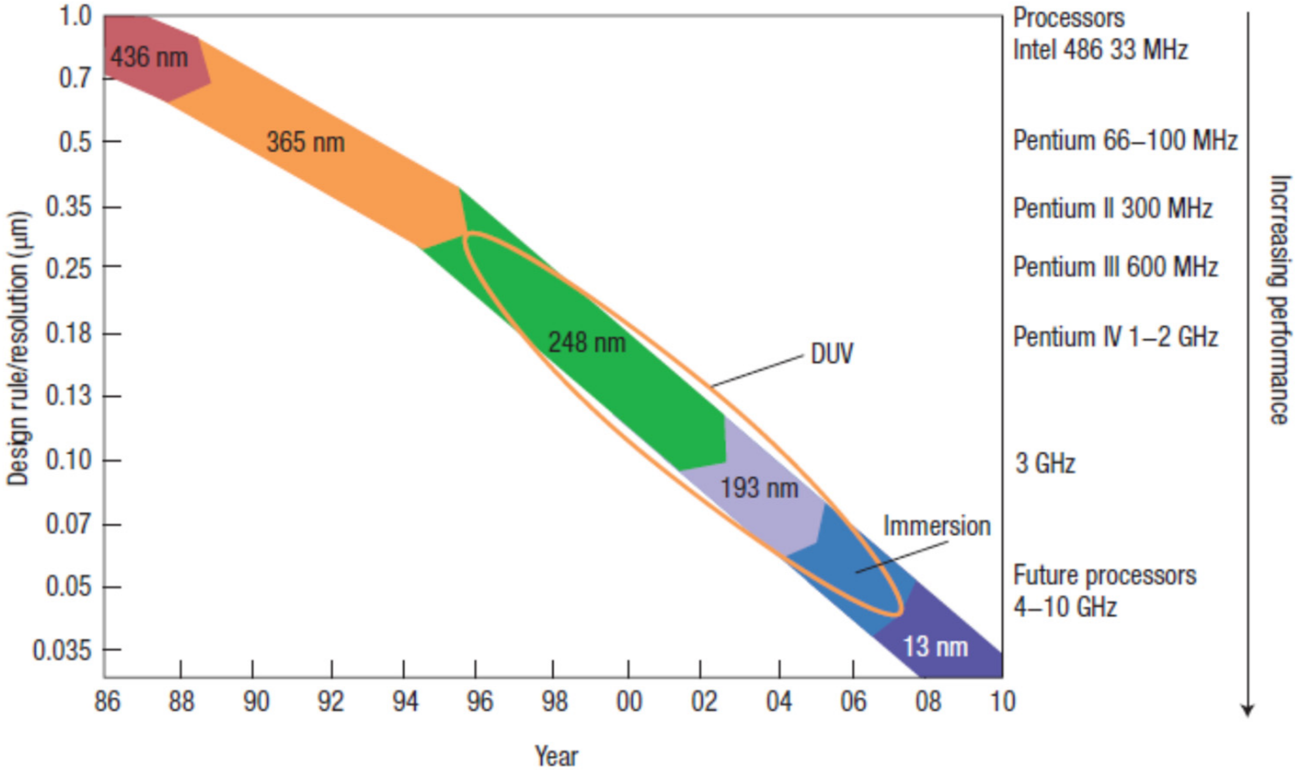


Fig. 2 (*a*) The wafer after the development. (*b*) The wafer after SiO_2 removal. (*c*) The final result after a complete lithography process. (*d*) A *p*–*n* junction is formed in the diffusion or implantation process. (*e*) The wafer after metallization. (*f*) A *p*–*n* junction after the complete processes.

Optical lithography



Speed/power tradeoff ⇒ CPU underclocking can save a lot of power while sacrificing much less the performance (motivation for multicore CPUs)

Example: Intel chips (2008), single core underclocking by 20% will save half the power for 13% less performance !

Optical lithography

The **fabrication of integrated circuits** (ICs) relies on **expensive photolithography systems**

Patterns optically imaged onto Si wafers covered with a photoresist

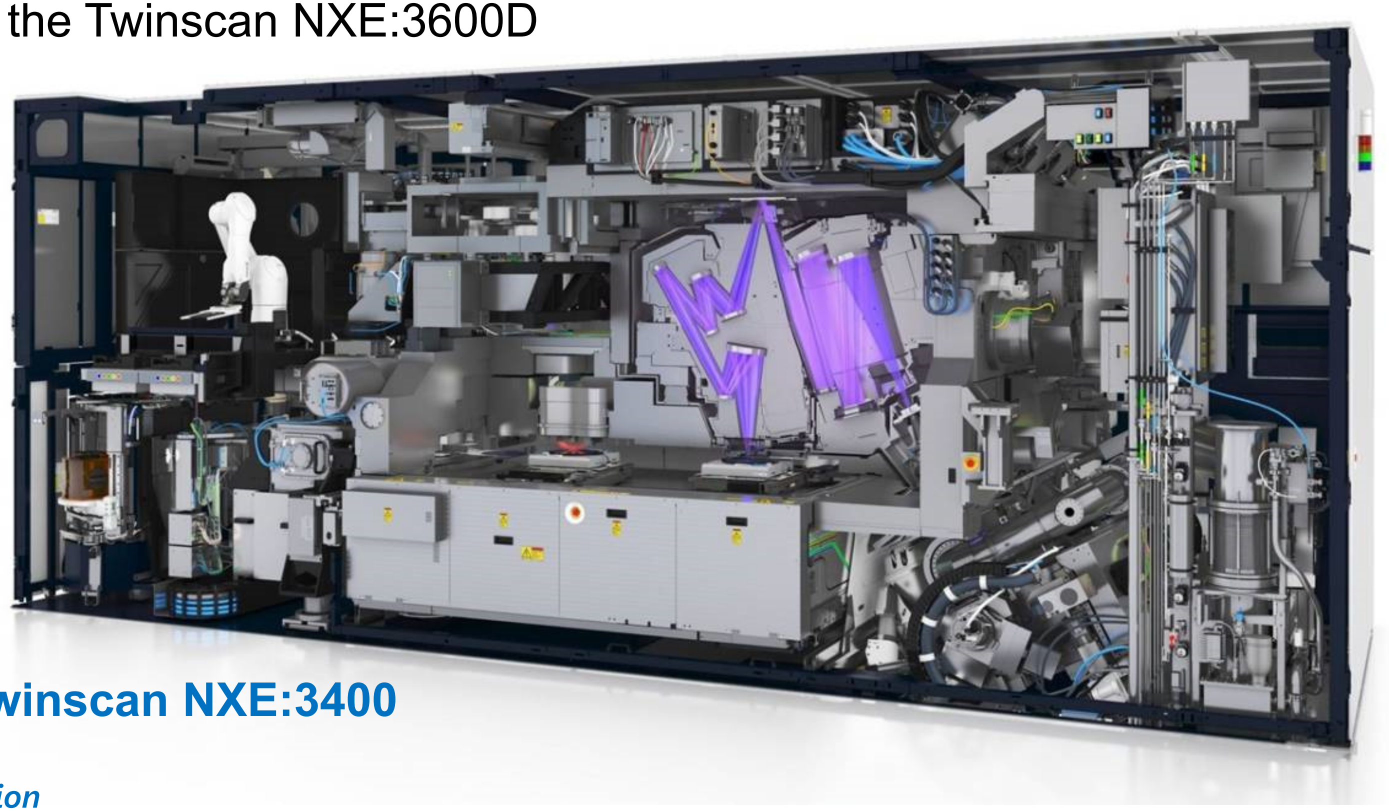
- Leading company: ASML (Dutch), >3/4 of the market ⇒ provider of immersion and EUV lithography machines (sole supplier of EUV tools, market capitalization in 2024 ~US$400 billion)
- Other players: Canon, Nikon, Ultratech (now part of Veeco Instr.) (USA)

Optical lithography machines set the transistor technology node, i.e., the typical half-pitch (≡ half distance between identical features in an array) for a memory cell.
22 nm technology node for the CMOS process, e.g., multicore processors. 14 nm technology node introduced by Intel at the end of 2014 (broad OEM, 2015)

Optical lithography

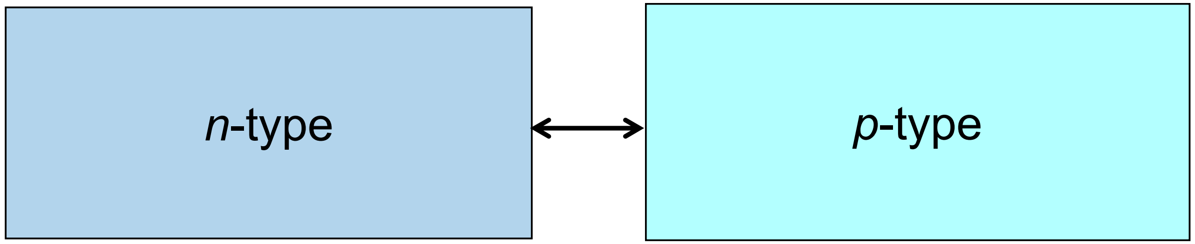
New generation of wafer stepper:

- Lens-free optical lithography
- All-mirror-based technology operating in the extreme UV (13.5 nm), hence under vacuum (to avoid air absorption)
- Used by Intel, IBM, Samsung and TSMC
- Cost up to 200 M$/unit for the Twinscan NXE:3600D



EUV lithography scanner – Twinscan NXE:3400

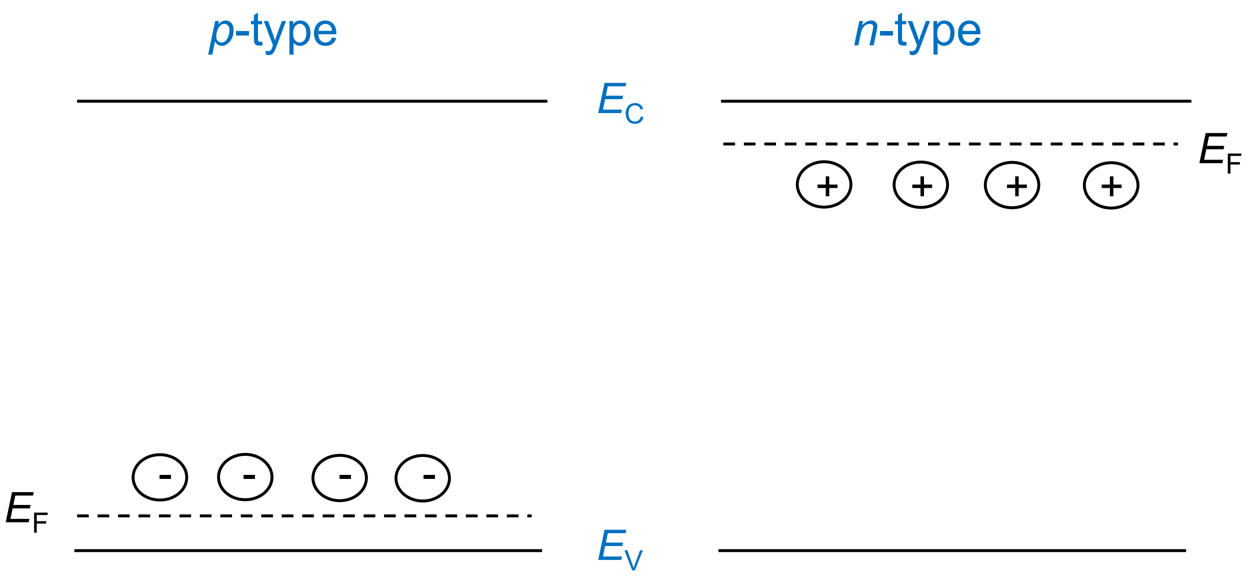
p-*n* junction: how does it work?



Case of the abrupt *p*-*n* junction (metallurgical junction)

Band diagram

- **At thermal equilibrium**



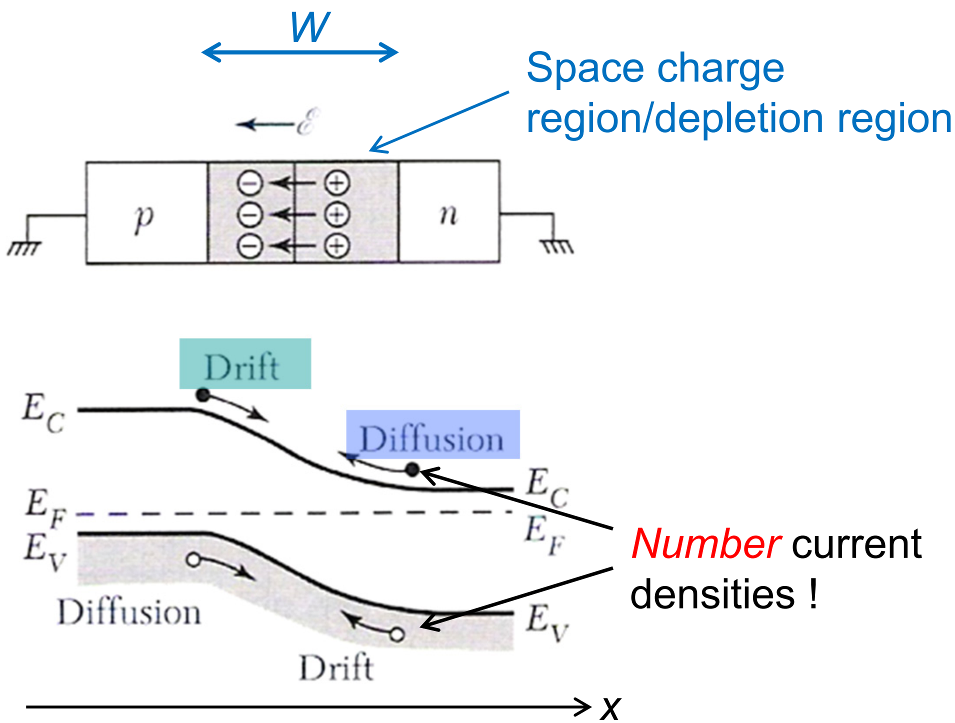
- Concentration gradients ⇒ diffusion currents
- Uncompensated ionized impurities ⇒ built-in electric field ⇒ drift currents

p-n junction at equilibrium

- Diffusion and drift currents

$\mathbf{J}_{\mathbf{n,drift}} = \sigma_n \mathbf{E} = e\mu_n n\mathbf{E}$

$\mathbf{J}_{\mathbf{n,diff}} = eD_n \,\mathbf{grad}\, n$



Einstein relation:

$$\frac{D}{\mu} = \frac{k_B T}{e}$$

Diffusion coefficient in $cm^2\ s^{-1}$

Link between *number* (*j*) and *electrical* (*J*) current densities:

$$\mathbf{J}_n = -e\mathbf{j}_n$$

and

$$\mathbf{J}_p = e\mathbf{j}_p$$

Band diagram

- **At thermal equilibrium**

The Fermi level is constant throughout the structure (details to be seen in the series)

$J_n = J_{n,\mathrm{drift}} + J_{n,\mathrm{diff}} = 0$ (also true for holes)

NO "net" current flowing through the junction

To be verified in the exercises

$$J_n = e\mu_n nE + eD_n \frac{dn}{dx} = \mu_n n \frac{dE_F}{dx} = 0$$

Keep in mind that Ohm's law is valid provided $v_d << v_{th}$!

1D case

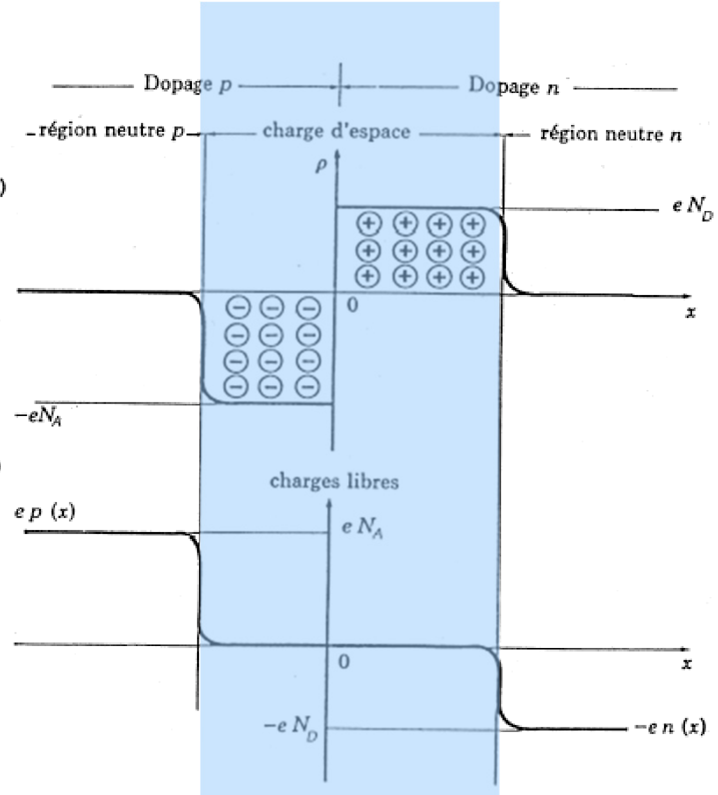
Full compensation between the drift and diffusion currents !

Band diagram

Space charge

Fixed charges

Mobile charges



Band diagram

- **At thermal equilibrium**

Built-in potential:

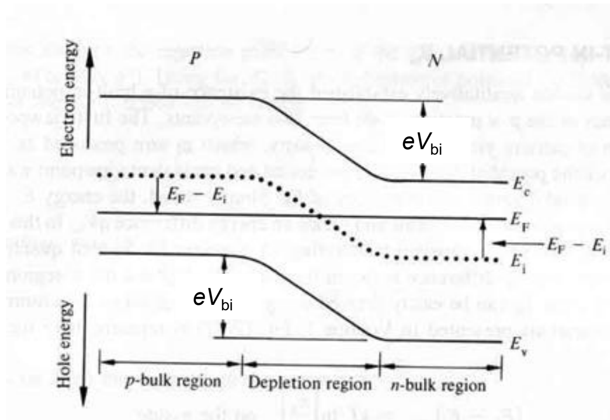
$eV_{bi} = (E_F - E_i)_n - (E_F - E_i)_p$ ≡ energy loss across the junction

with

$$E_F = E_c - k_B T \ln \frac{N_c}{n} = E_v + k_B T \ln \frac{N_v}{p}$$

$$p = N_v \exp\left[-(E_F - E_i)/k_B T\right] \exp\left[-(E_i - E_v)/k_B T\right] = n_i \exp\left[(E_i - E_F)/k_B T\right]$$

Similar treatment for electrons



($n \approx N_D$ and $p \approx N_A$)

If we consider that all impurities are ionized

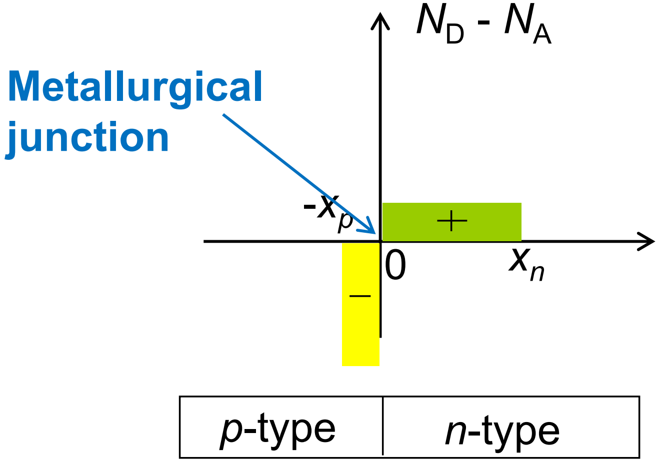
$$eV_{bi} = E_g - k_B T \ln\left(\frac{N_v N_c}{N_A N_D}\right)$$

Built-in barrier

This built-in potential V_{bi} is the consequence of the space charge due to carrier diffusion

Space charge region

Abrupt junction Poisson's equation to be solved as a function of position:



$$\frac{d^2\phi}{dx^2} = -\frac{\rho(x)}{\varepsilon_r \varepsilon_0}$$

Electrostatic potential vs position

$$\frac{d^2\phi}{dx^2} = e\frac{N_A}{\varepsilon} \quad for \quad -x_p \le x < 0 \qquad \varepsilon = \varepsilon_r \varepsilon_0$$

$$\frac{d^2\phi}{dx^2} = -e\frac{N_D}{\varepsilon} \quad for \quad 0 < x \le x_n \qquad \int_{-x_p}^{x_n} \rho dx = 0$$

Charge neutrality: $x_p N_A = x_n N_D$

Space charge region extent: $W = x_p + x_n$

Electric field in the space charge region

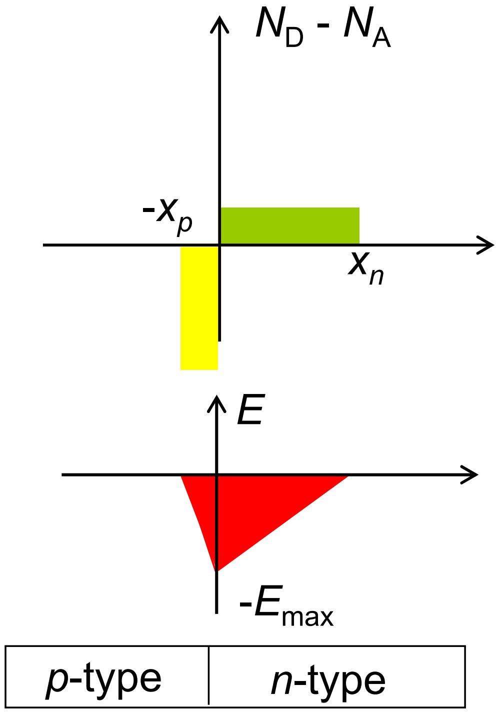
$$E(x) = -\frac{d\phi}{dx} = -e\frac{N_A(x+x_p)}{\varepsilon} \quad [-x_p, 0]$$

$$E(x) = -\frac{d\phi}{dx} = e\frac{N_D(x-x_n)}{\varepsilon} \quad [0, x_n]$$

$$|E_{max}| = e\frac{N_A x_p}{\varepsilon} = e\frac{N_D x_n}{\varepsilon}$$

Space charge region

Abrupt junction



$$V_{bi} = -\int_{-x_p}^{x_n} E(x)\,dx$$

$$= e\frac{N_A}{\varepsilon}\int_{-x_p}^{0}(x + x_p)\,dx - e\frac{N_D}{\varepsilon}\int_{0}^{x_n}(x - x_n)\,dx$$

$$= e\frac{N_A x_p^2}{2\varepsilon} + e\frac{N_D x_n^2}{2\varepsilon}$$

$$= \frac{E_{max} x_p}{2} + \frac{E_{max} x_n}{2} = \frac{1}{2}E_{max}W$$

Note that:

$$V_{bi} = \frac{1}{\varepsilon}\int_{-x_p}^{x_n}\left[\int_{-x_p}^{x}\rho\,dx\right]dx$$

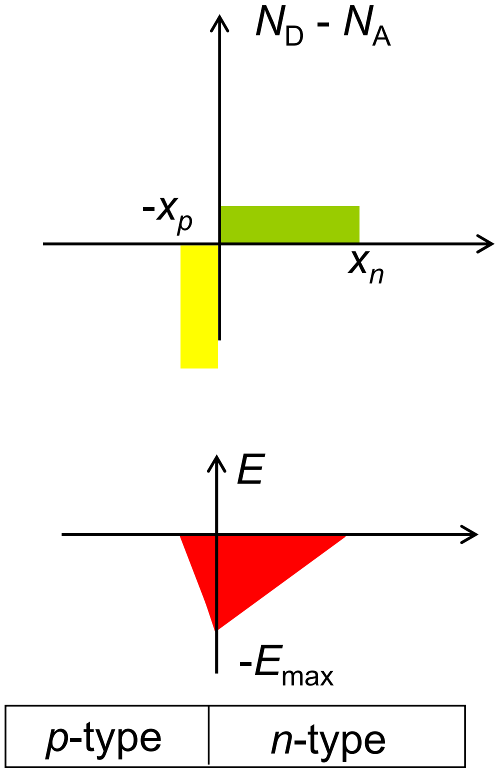
which can also be written:

Valid both at thermal equilibrium and out of equilibrium $\Rightarrow$

$$V_{bi} = \frac{1}{\varepsilon}\int_{-x_p}^{x_n} x\rho\,dx$$

Space charge region

Abrupt junction



$$V_{bi} = e\frac{N_A x_p^2}{2\varepsilon} + e\frac{N_D x_n^2}{2\varepsilon}$$

Charge neutrality: $x_p N_A = x_n N_D$

Space charge extent: $W = x_p + x_n$

⇨ $W = x_p\,(1+N_A/N_D) = x_p(N_D+N_A)/N_D$

$W = x_n \ldots$

$$W = \sqrt{\frac{2\varepsilon}{e}\left(\frac{N_A + N_D}{N_A N_D}\right)V_{bi}}$$

All the parameters entering into this expression are known beforehand!

Extent of the space charge region

Space charge region

Example: silicon-based *p-n* junction at 300 K

n-type: $N_D = 10^{18}$ cm^{-3} and $p = n_i^2/N_D = 10^2$ cm^{-3}

p-type: $N_A = 10^{18}$ cm^{-3} and $n = n_i^2/N_A = 10^2$ cm^{-3}

Cf. Lecture 6 ⇒ use of mass action law at thermal equilibrium + full ionization of impurities (+ charge neutrality condition)

$N_c = 2.7 \times 10^{19}$ cm^{-3} and $N_v = 1.1 \times 10^{19}$ cm^{-3}

We find:

eV_{bi} = 0.96 eV

$$eV_{bi} = E_g - k_B T \ln\left(\frac{N_v N_c}{N_A N_D}\right)$$

W = 50 nm

$$W = \sqrt{\frac{2\varepsilon}{e}\left(\frac{N_A + N_D}{N_A N_D}\right)V_{bi}}$$

$\varepsilon = \varepsilon_0 \varepsilon_r$

$\varepsilon_0 = 8.85 \times 10^{-12}$ F m^{-1}

$\varepsilon_r = 11.9$

$e = 1.6 \times 10^{-19}$ C

$E_{max} = 3.8 \times 10^5$ V cm^{-1}

$$E_{max} = 2V_{bi}/W$$

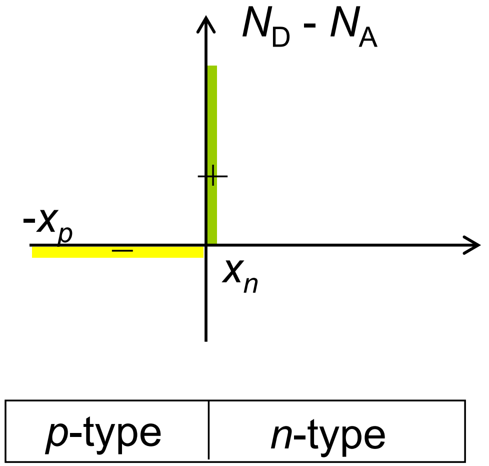
Other example: $N_A = N_D = 10^{15}$ cm^{-3}, eV_{bi} = 0.61 eV, W = 1.2 µm

Space charge region

Space charge in the *n*-type and *p*-type regions

$x_n = N_A/(N_D+N_A)W$

$x_p = N_D/(N_D+N_A)W$



If $N_D >> N_A$ then

$$W = \sqrt{\frac{2\varepsilon}{e}\frac{V_{bi}}{N_A}}$$

and $x_p = W$

One-sided abrupt junction approximation

The space charge mostly extends in the less doped region